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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**
**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**



Applicant(s): K. KATSURA, et al.

Serial No.: 07/985,141

Filing Date: December 3, 1992

For: GRAPHIC PROCESSING APPARATUS UTILIZING IMPROVED DATA TRANSFER TO REDUCE MEMORY SIZE

Group: 2772

Examiner: M. Zimmerman

## APPEAL BRIEF

Assistant Commissioner
for Patents
Washington, D.C. 20231

January 8, 1999

Sir:

This Appeal Brief is being filed in response to the decision by the Examiner in the Final Office Action dated December 8, 1997 and the Advisory Action of October 14, 1998 in which claims 44-66 were finally rejected.

## REAL PARTY IN INTEREST

The Real Party in Interest in this application is Hitachi, Ltd. as evidenced by an Assignment filed on April 5, 1989 in application Serial No. 07/302,332, filed January 27, 1989 and recorded at Reel 5061 and Frame 277.



## RELATED APPEAL AND INTERFERENCES

On information and belief, Appellants submit that there are no other appeals or interferences which will directly affect or be directly affected by or have any bearing on the Board's decision in the pending appeal.

## STATUS OF CLAIMS

Claims 44-66 stand rejected under 35 USC §251 as being based upon an alleged defective Reissue Declaration.

Claims 44-58 and 63-66 stand rejected under 35 USC §103 as being unpatentable over U.S. Patent No. 4,716,527 (Graciotti) in view of Japanese patent application 63-83844 (Takenaka) and U.S. Patent No. 4,796,231 (Pinkham).

## STATUS OF AMENDMENTS AFTER FINAL REJECTION

An Amendment After Final was filed on September 28, 1998 amending the claims to place them in better condition for Appeal. The September 28, 1998 Amendment After Final was entered by the October 14, 1998 Advisory Action.

## SUMMARY OF INVENTION

Appellants invention is directed to a graphic processing apparatus and a memory controller for controlling the transfer of data between memory and a data processor such that n bit data output from the data processor is input in successive groups of m bit data into the memory and successive groups of m bit data output from the memory are arranged in parallel so as to form n bit data which is then input to the data processor, wherein $n > m$.

Appellants invention is illustrated in Figs. 1 and 4 wherein the graphic processing apparatus includes a data processor 10, a memory controller 20 and memory 30. The data processor 10 is connected to the memory controller 20 through, for example, a data bus having a bit width of 16 bits. The

memory controller 20 is connected to the memory 30 through, for example, a data bus having a bit width of 4 bits.

The details of the memory controller are illustrated in Fig. 4 and the write, read and display operations are described on page 4, lines 9-51 of the application.

In the above-noted passage of Appellants' application, it is described that when a read operation is conducted successive read operations are conducted so as to read into the memory controller 20 successive groups of m bit data on data bus FD0-FD7. The successive groups of m bit data is stored in input data latch 2015, formed into n bit data and output to the data processor 10 on data bus MAD0-MAD15.

When a write operation is conducted the memory controller inputs n bit data from the data processor on data bus MAD0-MAD15 and stores the data in input data latch 2015. The n bit data is then read out in successive groups of n bit data to the memory 30 on data bus FD0-FD7.

When a display operation is to be conducted successive groups of m bit data is obtained from memory 30 through data bus FD0-FD7 and stored in input data latch 2015. Thereafter, the data is transferred to a display data latch 2019. The data stored in the display data latch 2019 is then output through various circuitry including a shifter 2020, a skew circuit 2022, a cursor blink circuit 2023, a multiplexer 2024 and a mask 2025 so as 1 bit serial video signal to a digital analog converter having built-in color pallet (CPLT) 40. CPLT 40 converts the 1 bit serial video signal into an analog video signal which is then supplied to a CRT 50 for display thereon.

Therefore, according to above description of Appellants' invention the graphic processing apparatus as recited in the claims includes a memory 30 for storing graphic data, a data processor 10 for executing a predetermined graphic processing to generating graphic data to be stored in the memory, output means 40 and 50 for outputting the graphic data read out from the memory and a memory controller 20 for controlling data transfer between memory and the data processor in accordance with their request from the data processor.

The memory controller as recited in the claims includes a storage 2015 for temporarily storing graphic data read out from the memory in successive groups of m bits of data, means for forming 2000-2011 n bits of data using the successive groups of m bits of data and supplying the n bits of data in parallel to the data processor and a converter 2019-2025 for converting the graphic data temporarily stored in the storage into serial data which is provided to the output means 40 and 50.

## ISSUES PRESENTED FOR REVIEW

Whether claims 44-66 are based on a defective Reissue Declaration under 35 USC §251.

Whether claims 44-58 and 63-66 are unpatentable over Graciotti in view of Takenaka and Pinkham under 35 USC §103.

## GROUPING OF CLAIMS:

Each of the claims of Appellants' application should be considered by the Board individually and separately so as to not stand or fall together.

**ARGUMENTS:**

With respect to the rejection of claims 44-66 as being based on an alleged defective Reissue Declaration under 35 USC §251 the following is provided:

A Supplemental Reissue Declaration was filed on September 28, 1998 which Appellants' submit fully comply with the requirements as now set forth in the revised Rules of Practice, particularly 37 CFR §1.175.

The Supplemental Reissue Declaration sets forth at least one error based upon which the Reissue application was being filed. It should be noted that there may be numerous other errors that are being corrected by the Reissue application, but only one needs to be listed. In the Supplemental Reissue Declaration, it is pointed out specifically that Appellants' believe:

> "the original patent to be wholly or partly inoperative or invalid by defective specification and claiming less and/or more than we had a right to claim in the patent" (Emphasis added)

Thus, there are several alternative errors causing the patent to be wholly or partly inoperative, namely a defective specification and claiming less than they had a right to claim in the patent and/or a defective specification and claiming more than they had a right to claim in the patent. Thereafter, in the Supplemental Reissue Declaration, the one error being described is where Applicants claimed less than they had a right to claim. In other words, the error was that the claims could have been drafted more broadly. This error

contrary to the Examiner's allegation is embodied in the currently pending claims particularly, when for example, claims 59 and 63 are viewed relative to the claims 1-8 set forth in the granted patent. Claims 1-8 set forth in the granted patent are directed to, for example, a graphic processing apparatus having memory means, data processing means, memory control means, memory data bus and processor data bus. There are no claims set forth in the granted patent which are directed to only the memory controller as recited in claims 59 or 63 without the other elements of the graphic processor and the memory as set forth in claims 1-8 of the granted patent.

It is respectfully submitted that a reasonably skilled practitioner could readily recognized that a claim to a memory controller would be infringed by and is therefore broader than a claim to a graphic processing apparatus including the memory controller, data processing apparatus and memory. Thus, at least one of the claims of Appellants' application is broader than claims 1-8 set forth in the granted patent. Therefore, it would appear that claims 59 and 63 are broader in some respects relative to the claims of the granted patent contrary to the allegation set forth by the Examiner.

Further, even when viewing the other claims of Appellants' application, they are broader in some respects relative to the claims of the granted patent and, at the same time, narrower in other respects relative to the claims of the granted patent. Thus, here again, since the error lies in not drafting the claims more broadly, then the inclusion of claims

which are broader in some respects relative to the claims of the granted patent in an attempt to correct the error set forth in the Reissue Declaration.

Accordingly, it is completely appropriate to recite that one of the errors is that the claims were not claimed as broadly as they should have been claimed being that this is merely one of the many errors to be corrected by the Reissue patent application, and that such broader claims are included in the pending claims.

Even beyond the above, the Examiner seems to completely disregard the clear language used in the Supplemental Reissue Declaration. Attention is directed to the placement and use of the term "and/or". This term allows for the possibility where at least one or both of the following errors could exist (1) defective specification and claiming less than they had a right to claim and (2) a defective specification and claiming more than they had a right to claim. Accordingly, any one or both of these errors could exist permitting the Supplemental Reissue Declaration to be effective in any of the listed situations under 35 USC §251. Thus, for example, if only an error regarding a defective specification and claiming more than they had a right to claim was corrected the Supplemental Declaration would still be effective, since this is are merely an alternative error.

Appellants' fail to understand why the Examiner has not fully read nor made any effort to understand the language as set forth in the Supplemental Reissue Declaration and the practice as now set forth under 37 CFR §1.175 and chooses to

force Appellants' to Appeal such a minor issue to the Board.

Appellants' respectfully request the Board to reverse the rejection of the claims under 35 USC §251.

With respect to the rejection of claims 44-58 and 63-66 under 35 USC §103 as being unpatentable over Graciotti in view of Takenaka and Pinkham the following is provided:

Appellants' submit that the features of the Appellants' invention as recited in claims 44-58 and 63-66 are not taught or suggested by Graciotti, Takenaka and Pinkham whether taken individually or in combination with each other as suggested by the Examiner. Graciotti is merely directed to the conversion of a 16 bit data bus to an 8 bit data bus so as to allow connection of a processor having a 16 bit data bus to a peripheral having an 8 bit data bus. Specifically, Graciotti teaches in Fig. 1 thereof a bus converter circuit which allows for a 16 bit data bus microprocessor to be compatible with peripheral devices designed for an 8 bit data bus. Graciotti teaches that in response to a particular command the bus converter circuit allows for the transfer between a microprocessor and a peripheral 16 bit data which is converted to 8 bit data for use by the peripheral.

Appellants' invention as clearly recited in the claims differs substantially from that taught by Graciotti being that the present invention is directed to <u>a graphic processing apparatus having a memory controller connected between a data processor and memory and the memory controller</u> itself. The memory controller as clearly recited in the claims and as disclosed in the specification is intended to perform control

operations of a memory to allow a data processor to access memory. The bus converter circuit taught by Graciotti is intended to be connected between a microprocessor and peripheral which as discussed in Graciotti can be software or a device such as a floppy disk controller as discussed in col. 2, lines 9-14 of Graciotti. The bus converter circuit as taught by Graciotti is not intended to be connected in a data processing system between memory and data processor as recited in the claims of Appellants' application. Even more particularly, the bus converter taught by Graciotti is not a memory controller as recited in the claims wherein the memory controller performs and provides all of the signals necessary for controlling the operation of memory as in Appellants' invention.

Further, Graciotti fails to teach or suggest the successive retrieval from memory of successive groups of m bits of data during a predetermined period of time as recited in the claims. In Appellants' invention as illustrated, for example, in Fig. 6 thereof the successive groups of m bits of data are retrieved from memory, for example, during a single memory cycle (MCYC, single access). Such is clearly not taught or suggested by Graciotti. The apparatus taught by Graciotti does not teach or suggest that the operation performed by the bus converter circuit is intended to occur within a single memory read or write cycle as in Appellants' invention.

Further, Appellants' fail to find any teaching or suggestion in Graciotti of the converter for converting the

graphic data temporarily stored in the storage into serial data which is provided to the output means based on an indication from the data processor as recited in the claims. As described above in the Summary of the Invention, the converter corresponds to the display latch 2019, shifter 2020, skew 2022, cursor blink 2023, multiplexer 2024 and mask 2025 and the output means corresponds to the CPLT 40. The converter converts the parallel data stored in input data latch 2015 into serial data which is supplied to CPLT 40. The CPLT 40 converts, for example, the serial video signal into an analog video signal which is then output to CRT 50. The converter recited in the claims is clearly not taught or suggested by Graciotti.

The above described deficiencies of Graciotti are not supplied by Takenaka and Pinkham. Takenaka merely describes a microprocessor system having added hardware for automatically converting a word transfer command into byte transfer commands plural times. Takenaka teaches that a word transfer command is produced from a microprocessor 1 and a timing generator circuit 7 checks whether the word transfer command starts at an even address and the object of the command is a ROM having data of an 8 bit width. Takenaka teaches that two bytes of the ROM can be retrieved by incrementing a counter which increases by one the address corresponding to the word transfer command.

Appellants' fail to find any of the above described features regarding the graphic processing apparatus having a memory controller connected between a data processor and

memory; the memory controller itself; successive retrieval from memory successive groups of m bits of data during a predetermined period of time and a converter in Takenaka. Particularly, Appellants' fail to find any teaching or suggestion in Takenaka of the converter as recited in the claims. The converter as described above converts graphic data temporarily stored in the storage into serial data which is provided to the output based on an indication from the data processor. As described above data stored in input data latch 2015 is provided to the display data latch 2019 as parallel data. The parallel data is then retrieved from the display data latch 2019 by the shifter 2020 and serial data is output from the video terminal to the CPLT 40. The CPLT 40 converts the serial data into analog data which is then supplied to the CRT 50. The CPLT 40 corresponds to the output means and the converter corresponds to the circuitry included in the memory controller such as, for example, the display data latch 2019, the shifter 2020 and the other circuits 2022-2025. These circuits are clearly not taught or suggested by Takenaka.

Even further, the above-described features shown to be deficient in Graciotti and Takenaka are not taught or suggested by Pinkham. Pinkham merely teaches a serial access semiconductor memory with reconfigurable shift registers. Pinkham teaches that each of the shift registers can be connected in a circulating fashion so that data loaded in parallel can be output in a serial format. Although Pinkham teaches the conversion of parallel data to serial data Appellants' fail to find any teaching or suggestion in Pinkham

that such circuitry can be used in a memory controller as recited in the claims of Appellants' application. Thus, Pinkham is deficient of numerous features of Appellants' invention the same as Graciotti and Takenaka. Therefore, the combination of Graciotti, Takenaka and Pinkham fails to teach or suggest the features of Appellants' invention as recited in the claims.

In fact, Appellants' submit that the references Graciotti, Takenaka and Pinkham cannot be combined in the manner as alleged by the Examiner being that the Examiner has not pointed to any objective teaching in any of the references that describe or even hint that such a combination can be made.

It appears that the Examiner is using hindsight in order to meet the features of Appellants' invention as recited in the claims. To substitute for such glaring omission the Examiner makes various unsupported allegations as to where the suggestion of such combinations can be found. However, upon complete and full review of such passages in the references, it is quite clear that the Examiner is merely making unsupported allegations which have no basis in any of the references of record nor are the allegations appropriate when making a *prima facia* case of obviousness. In fact, the Examiner admits on numerous occasions of the lack of teachings in the references of record of specific features recited in the claims.

For example, the Examiner admits that Graciotti does not disclose the claimed conversion means. However, the Examiner

alleges that such is known in the art as taught by Pinkham. Appellants' fail to find any teaching whatsoever in Pinkham of conversion means as recited in the claims. Further, the connections and the purposes behind the respective circuits disclosed by Graciotti and Pinkham are entirely different. Thus, one of ordinary skill in the art would not have been lead by any teaching in Graciotti or in Pinkham to combine the respective circuits thereof in the manner as alleged by the Examiner. The Examiner seems to be merely making allegations to support a failed attempt to make a *prima facia* case of obviousness under 35 USC §103.

Particularly, the Examiner has failed to show in any of the references of record of a converter corresponding to, for example, the circuits 2019-2025 included in the memory controller 20 as illustrated in Figs. 1 and 4 wherein graphic data temporarily stored in the storage 2015 is converted into serial data which is provided to output means CPLT 40 based on an indication from the data processor. Such an element is clearly not taught or suggested by Graciotti, Takenaka or Pinkham whether taken individually or in combination with each other.

Throughout the prosecution the Examiner has made broad statements as to what one of ordinary skill in the art would have known in order to modify the teachings of the Graciotti, Takenaka and Pinkham references in order to meet the limitations of Appellants' invention as recited in the claims. These modifications alleged by the Examiner to have been known by one of ordinary skill in the art are merely fabrications on

the part of the Examiner using his current understanding. The fabrications are not supported by any teaching in any of the references of record.

Further, the alleged knowledge by one of ordinary skill in the art proffered by the Examiner has not been related by the Examiner to what would have been known by one of ordinary skill in the art at the time of Appellants' invention. The Examiner's allegation of knowledge and modifications that one of ordinary skill in the art would make to the references of record are all based on the Examiner's current knowledge, not knowledge existing prior to Appellants' invention.

In fact the Examiner is relying upon the teachings in Appellants' disclosure in order to make the combination (hindsight). Had it not been for the disclosure in Appellants' application the Examiner nor one of ordinary skill in the art would have been led to combine the references in the manner alleged by the Examiner since no evidence that such a combination can be made exists.

One particular combination that the Examiner alleges can be made that seems particularly impossible is the combining of Graciotti with Pinkham in order to provide a converter as recited in each of the claims. The Examiner recognizes that "Graciotti does not explicitly disclose the claimed conversion means". However, the Examiner alleges that such is known in the art as taught by Pinkham. However, the disclosure pointed to by the Examiner in Pinkham could not have been combined with the Graciotti circuitry in the manner alleged by the Examiner since the connections are totally incompatible and

the purposes behind each of the respective circuits disclosed by Graciotti and Pinkham are entirely different.

The combination alleged by the Examiner can not be made and is merely the Examiner's fabrication not supported by either of the disclosures. Here it is particularly obvious that the Examiner is merely relying on Appellants' disclosure which provides the need for a converter. The Examiner then finds Pinkham, allegedly having a teaching of a converter, to supply the need for a converter as set forth in Appellants' invention. The need for a converter arose in Appellants' invention not in Graciotti since it was never Graciotti's intention to provide a memory controller that operates in combination with a data processor, memory and an output device such as a CRT as in Appellants' invention. Thus, the Examiner is being improperly guided by Appellants' disclosure. The Board is respectfully requested to correct the Examiner on this point.

Further, the alleged converter in Pinkham does not perform the conversion recited in the claims of Appellants' application. The conversion recited in the claims of Appellants' application provides for the conversion of the graphic data temporarily stored in the storage of the memory controller into serial data which is provided to an output means. This element corresponds to circuits 2015-2025 illustrated in Fig. 1 of Appellants' application. The alleged converter in Pinkham does not perform such a function nor is it intended to be combined with apparatus such as that taught in Graciotti. Therefore, the combination as alleged by the

Examiner would be impossible.

Claim 45 depends from claim 44 and recites that the memory controller further includes a multiplexer for outputting the n bits of data transferred from the data processor to the first bus having n bits within successive groups of n bits of data during the predetermined period of time. The Examiner has not shown where any such multiplexer can be found in any of the references of record nor is it taught or suggested by the references of record.

Claim 46 which depends from claim 44 recites that the memory controller further includes means for generating an address signal for accessing the memory plural times in response to a signal for accessing the memory supplied from the data processor to obtain successive groups of n bits of data. Such a means for generating an address signal for accessing the memory plural times has not been addressed by the Examiner nor is it taught or suggested by any of the references of record.

Claim 47 which depend from claim 44 recites that the successive groups of n bits of data to be transferred to the memory controller through the first bus is read out by accessing the memory plural times within a unit transfer time based on an access signal to the memory designated by the data processor. Such a feature has not been addressed by the Examiner nor is it taught or suggested by any of the references of record.

Claim 48 which depend from claim 47 recites that the successive groups of n bits of data transfer to the memory

controller through the first bus is combined to form n bits of data supplied to the data processor through the second bus within a time longer than twice the unit transfer time. This feature have not been addressed by the Examiner nor is it taught or suggested by the references of record.

Claim 50 which depends from claim 49 recites that the memory controller includes a multiplexer for outputting n bit graphic data transfer from the data processing means on the first bus having the m bit width successively in a time sharing manner. The Examiner has not addressed this feature nor is it taught or suggested by the references or record.

Claim 51 which depend from 49 recites that the memory controller includes means for generating address signals for accessing the memory means plural times with respect to a signal for accessing the memory means plural times with respect to a signal for accessing the means applied from the data processing means. The Examiner has not addressed this feature nor is it taught or suggested by any of the references of record.

Claim 52 which depends from claim 50 recites that the memory controller includes means for generating address signal for accessing the memory means plural times with respect to a signal for accessing the memory means plural times with respect to a signal for accessing the memory means applied from the data processing means. The Examiner has not addressed this feature nor is it taught or suggested by any of the references of record.

Claim 53 which depends from claim 49 recites that the

graphic data to be transferred to the memory controller via the first bus are successively read out plural times within a transfer unit time in a predetermined period of time on the basis of an access signal to the memory means designated by the data processing means. The Examiner has not addressed this feature nor is it taught or suggested by any of the references of record.

Claim 54 which depends from claim 50 recites that the graphic data to be transferred to the memory controller via the first bus are successively read out plural times with a transfer unit time in a predetermined period of time on the basis of an access signal to the memory means designated by the data processing means. The Examiner has not addressed this feature nor is it taught or suggested by any of the references of record.

Claims 55 and 56 which depends respectively from claims 53 and 54 recites the same features wherein graphic data transferred to the memory controller are applied to the data processing means via the second bus within a time period more than two times the transfer unit time. The Examiner has not addressed this feature nor is it taught or suggested by any of the references of record.

Claim 58 which depend from claim 57 recites that the memory controller includes means for successively generating a plurality of column addresses on the basis of a signal for accessing the memory means applied from the data processing means. The Examiner has not addressed this feature nor is it taught or suggested by any of the references or record.

Claim 64 which depend from claim 63 recites that the successive groups of m bits of data from the m bit terminals are read out of the memory by performing plural read operation within a memory cycle based on an address specified by the processor. This feature has not been addressed by the Examiner nor is it taught or suggested by any of the references of record.

Claim 65 recites that the n bits of data is supplied to the processor through the n bit terminals in a unit of time more than two times the memory cycle. This feature has not been addressed by the Examiner nor is it taught or suggested by any of the references of record.

Claim 66 recites that the successive groups of n bits of data each include an m bit portion of the n bits of data. This feature has not been addressed by the Examiner nor is it taught or suggested by any of the references of record.

Even beyond the above, the Examiner has not addressed nor has the Examiner shown where each of the different features of the invention recited in the independent claims are taught or suggested by the referenced of record. For example, claim 44 recites that the memory controller includes means for forming n bits of data using the successive groups of m bits of data and supplying the n bits of data in parallel to the data processor through the second bus based on an indication from the data processor. Whereas, claim 49 recites that the memory controller includes means for applying the temporarily stored graphic data to the data processing unit as n bit parallel data based on an indication from the data processor means.

The differences between claims 44 and 49 have not been addressed by the Examiner nor are they taught or suggested by the references of record.

Claim 57 differs even further from claims 44 and 49 being that claim 57 recites that the memory controller includes means for reading out a plurality of graphic data at different column addresses at a same row address from the memory means via a first bus successively in a predetermined period of time. The Examiner has not addressed these features recited in claim 57 nor has the Examiner pointed to where the differences between claims 44, 49 and 57 can be found in the references of record.

Further, as described above independent claim is directed to a memory controller which at no point during the prosecution been addressed by the Examiner. The memory controller recited in claim includes m bit terminal, n bit terminals, a storage, means for forming n bits of data by combining successive groups of n bits of data and converting means for converting graphic data temporarily stored in the storage into serial data which is supplied to output means. At no point during the prosecution has the Examiner addressed these features

nor are they taught or suggested by any of the references or record.

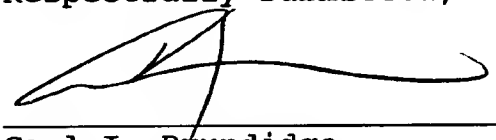
**SUMMARY**

Appellants' submit that the Examiner's final rejection of

the claims under 35 USC §251 as being based on an alleged defective Reissue Declaration and under 35 USC §103 as being unpatentable over Graciotti, Takenaka and Pinkham are not properly founded in law and respectfully request that the Board reverse the Examiner's final rejection.

To the extent necessary, applicants petition for an extension of time under 37 C.F.R. section 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (Case No. 500.26967R00) and please credit any excess fees to such Deposit Account.

Respectfully submitted,



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## APPENDIX

CLAIMS

44. A graphic processing apparatus comprising:

a memory for storing graphic data;

a data processor for executing a predetermined graphic processing to generate graphic data to be stored in said memory;

output means for outputting said graphic data read out from said memory;

a memory controller for controlling data transfer between said memory and said data processor in accordance with a request from said data processor;

a first bus, having m (wherein m is an integer) bits width, connected between said memory and said memory controller, for transferring m bits of data in parallel; and a second bus, having n (wherein n is an integer, n > m) bits width, connected between said memory controller and said data processor, for transferring n bits of data in parallel;

wherein said memory controller comprises:

a storage for temporarily storing graphic data read out from said memory in successive groups of m bits of data during a predetermined period of time through said first bus,

means for forming n bits of data using said successive groups of m bits of data and supplying said n bits of data in parallel to said data processor through said second bus based on an indication from said data processor, and

a converter for converting said graphic data temporarily stored in said storage into serial data which is provided to said output means based on an indication from said

data processor.

45. An apparatus according to claim 44, wherein said memory controller further comprises:

a multiplexer for outputting the n bits graphic data transferred from said data processor to said first bus having m bits width in a time shared fashion.

46. An apparatus according to claim 44, wherein said memory controller further comprises:

means for generating an address signal for accessing said memory plural times, in response to a signal for accessing said memory supplied from said data processor.

47. An apparatus according to claim 44, wherein graphic data to be transferred to said memory controller through said first bus is read out from said memory plural times within a unit transfer time in a time shared fashion, based on an access signal to said memory designated by said data processor.

48. An apparatus according to claim 47, wherein the graphic data transferred to said memory controller is supplied to said data processor through said second bus within a time longer than twice said unit transfer time.

49. A graphic processing apparatus comprising:

memory means for storing graphic data;

data processing means for executing predetermined graphic processing to generate graphic data;

output means for outputting graphic data stored in said memory means;

a memory controller for controlling transfer of data between said memory means and said data processing means in response to a request from said data processing means;

a first bus having an m-bit width (wherein m is an integer) and connected between said memory means and said memory controller, for transferring data of m bits in parallel; and

a second bus having an n-bit width (wherein n is an integer and n>m) and connected between said memory controller and said data processing means, for transferring data of n bits in parallel,

wherein said memory controller includes:

storage means for temporarily storing graphic data read out from said memory means successively in a predetermined period of time via said first bus,

means for applying said temporarily stored graphic data to said data processing means as n-bit parallel data based on an indication from said data processing means, and

converting means for converting said temporarily stored graphic data into serial data and outputting the serial data to said output means based on an indication from said data processing means.

50. A graphic processing apparatus according to claim

49, wherein said memory controller includes multiplexer means for outputting n-bit graphic data transferred from said data processing means on said first bus having the m-bit width successively in a time-sharing manner.

51. A graphic processing apparatus according to claim 49, wherein said memory controller includes means for generating address signals for accessing said memory means plural times with respect to a signal for accessing said memory means applied from said data processing means.

52. A graphic processing apparatus according to claim 50, wherein said memory controller includes means for generating address signals for accessing said memory means plural times with respect to a signal for accessing said memory means applied from said data processing means.

53. A graphic processing apparatus according to claim 49, wherein graphic data to be transferred to said memory controller via said first bus are successively read out plural times within a transfer unit time in a predetermined period of time on the basis of an access signal to said memory means designated by said data processing means.

54. A graphic processing apparatus according to claim 50, wherein graphic data to be transferred to said memory controller via said first bus are successively read out plural times within a transfer unit time in a predetermined period of

time on the basis of an access signal to said memory means designated by said data processing means.

55. A graphic processing apparatus according to claim 53, wherein graphic data transferred to said memory controller are applied to said data processing means via said second bus within a time period more than two times said transfer unit time.

56. A graphic processing apparatus according to claim 54, wherein graphic data transferred to said memory controller are applied to said data processing means via said second bus within a time period more than two times said transfer unit time.

57. A graphic processing apparatus comprising:

memory means for storing graphic data, said memory means being accessed by using a row address and a column address;

data processing means for executing predetermined graphic processing to generate graphic data;

output means for outputting graphic data stored in said memory means;

a memory controller for controlling transfer of data between said memory means and said data processing means in response to a request from said data processing means;

a first bus having an m-bit width (wherein m is an integer) and connected between said memory means and said

memory controller, for transferring data of m bits in parallel; and

a second bus having an n-bit width (wherein n is an integer and n>m) and connected between said memory controller and said data processing means, for transferring data of n bits in parallel; and

wherein said memory controller includes:

means for reading out a plurality of graphic data at different column addresses at a same row address from said memory means via said first bus successively in a predetermined period of time,

means for applying said read-out graphic data to said data processing means as n-bit parallel data based on an indication from said data processing means, and

converting means for converting said read-out graphic data into serial data and outputting the serial data to said output means based on an indication from said data processing means.

58. A graphic processing apparatus according to claim 57, wherein said memory controller includes means for successively generating a plurality of column addresses on the basis of a signal for accessing said memory means applied from said data processing means.

59. A memory controller for controlling transfer of data between memory means for storing graphic data and a processor and between said memory means and display means, comprising:

m-bit terminals (wherein m is an integer) connected to said memory means, for transferring data of m bits successively in a predetermined period of time between said memory means and said memory controller;

an n-bit interface (wherein n is an integer and n>m) connected to said processor, for transferring data of n bits in parallel between said processor and said memory controller based on an indication from said processor;

at least one bit terminal connected to said display means, for transferring serial data between said display means and said memory controller;

first converting means for performing conversion between data of plural sets of m bits via said m-bit terminals and data of n bits via said n-bit interface based on an indication from said processor; and

second converting means for converting said data of plural sets of m bits via said m-bit terminals into said serial data.

60. A memory controller according to claim 59, wherein data to be converted by said first converting means are read out plural times from said memory means within a transfer unit time successively in a predetermined period of time on the basis of addresses designated by said processor.

61. A memory controller according to claim 59, wherein said first converting means includes storage means for

temporarily storing graphic data sent from said memory means via said m-bit terminals.

62. A memory controller according to claim 59, wherein said second converting means includes storage means for temporarily storing graphic data sent from said memory means via said m-bit terminals.

63. A memory controller for controlling transference of data between a memory and a processor, said memory controller comprising:

m bit terminals for coupling to said memory, wherein successive groups of m bits of data is transferred through said m bit terminals between said memory and said controller by performing plural read operations within a memory cycle (where m is an integer);

n bit terminals for coupling to said processor, wherein n bits of data is transferred in parallel through said n bit terminals between said controller and said processor (where n is an integer and n>m);

storage for temporarily storing graphic data read out from said memory in successive groups of m bits of data during a predetermined period of time through said m bit terminals;

means for forming n bits of data by combining successive groups of m bits of data from said m bit terminals and supplying said n bits of data in parallel to said n bit terminals based on an indication from said processor; and

converting means for converting said graphic data temporarily stored in said storage into serial data which is supplied to output means, said output means outputs graphic data read out from said memory based on an indication from said processor.

64. A memory controller according to claim 63, wherein said successive groups of m bits of data from said m bit terminals are read out of said memory by performing plural read operations within a memory cycle based on an address specified by said processor.

65. A memory controller according to claim 64, wherein said n bits of data is applied to said processor through said n bit terminals in a unit of time more than two times said memory cycle.

66. A memory controller according to claim 63, wherein said successive groups of m bits of data each includes an m bit portion of said n bits of data.